AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on page 2, line 16 as follows:

– In accordance with another broad aspect, the invention provides a method for generating a signal for transmission over a link between two ICs. An input signal is received, the input signal comprising payload data to be transmitted over the link between two ICs. The data in the input signal is processed to derive forward error correction data at least ~~on~~ in part on the basis of the payload data in the input signal. An output signal comprising the payload data received in the input signal and the forward error correction data is then generated and released for transmission over the link between two ICs. --

Please amend the paragraph beginning on page 4, line 2 as follows:

– It will be readily ~~appreciate~~ appreciated that any suitable coding may be applied to the payload data in a given block to derive the forward error correction data for that given block. In a very specific non-limiting example, the forward error correction data in a given primary data structure are derived by applying BCH-1 coding on at least part of the payload data of the given primary data structure. The skilled person in the art will readily appreciate that methods, other than BCH-1 coding, may be used in connection with FEC without detracting from the spirit of the invention. --

Please amend the paragraph beginning on page 7, line 27 as follows:

--The payload data may be ~~comprisees~~comprised of N channels or of a single channel. This specific example considers the case where the input signal is comprises of N channels. Each of the N channels is directed to a respective FEC calculator unit 200 202 204 206. At each FEC calculator unit, forward error correction data is computed on the basis of payload data. Many different FEC schemes may be used here. In a very specific example of implementation, the FEC

scheme is a 1rst order Binary BCH code. Advantageously, this FEC scheme allows the FEC decoder at the receiver to correct up to 1 error per primary data structure. Each FEC calculator unit then generates a primary data structure. Each primary data structure comprises a first portion and a second portion, the first portion including payload data, the second portion including forward error correction data derived from the data elements in the first portion. A representation of a specific implementation of the primary data structure is depicted in figure 3. In the specific implementation depicted in figure 3, each primary data structure includes 1176 bits. In the primary data structure 300, the payload data 302 occupies bits 1-1164, the forward error correction data 304 occupies 12 bits namely bits 1165-1176. --

Please amend the paragraph beginning on page 11, line 4 as follows:

-- Figure 5 shows a specific example of a digital signal frame format providing forward error correction. The frame 500 ~~and~~ includes 66 compound data structure blocks 510 and a framing pattern 512. Each block 510 in the frame 500 is characterized by a compound data structure of the type depicted in figure 4. At the beginning of each frame, a framing pattern is appended and is designated with reference numeral 512. It will be readily apparent that the framing pattern may alternatively be appended anywhere in the frame without detracting from the spirit of the invention. The framing pattern 512 occupies 72 bytes and is a fixed pattern used to identify frame boundaries. The frames generated by the frame generation unit are then forwarded to the transmit interface 110. --

Please amend the paragraph beginning on page 12, line 31 as follows:

-- The processing unit 602 processes the signal received from the receive interface [[110]] 610 to extract payload data to be transmitted to one or more functional processing units. The output 614 is for transmitting payload data extract3ed by the processing unit 602 to one or more functional processing units. --

Please amend the paragraph beginning on page 14, line 19 as follows:

– The FEC processing units 700 702 704 706 receive respective primary data structures. Each FEC processing ~~units~~unit decodes the FEC portion of the primary data structure and effects any required correction to the payload data portion. The specific FEC decoding function applied by the FEC processing units is dependent upon the FEC coding used by FEC calculator units 200 202 204 and 206. Advantageously, the use of FEC over a link between two ICs allows a reduction in the bit error rate (BER) when transmitting a signal over a backplane or between two ICS on a same circuit pack. The FEC processing units 700 702 704 706 then release a signal including payload data to output 614. The skilled person in the art will readily appreciate that different types of payload data may be released at output 614 without detracting from the spirit of the invention. –

Please amend the paragraph beginning on page 15, line 17 as follows:

– The apparatuses 100 may form part of an integrated circuit ~~imbeddedembedded~~ in a dedicated chip or may form part of an IC. –